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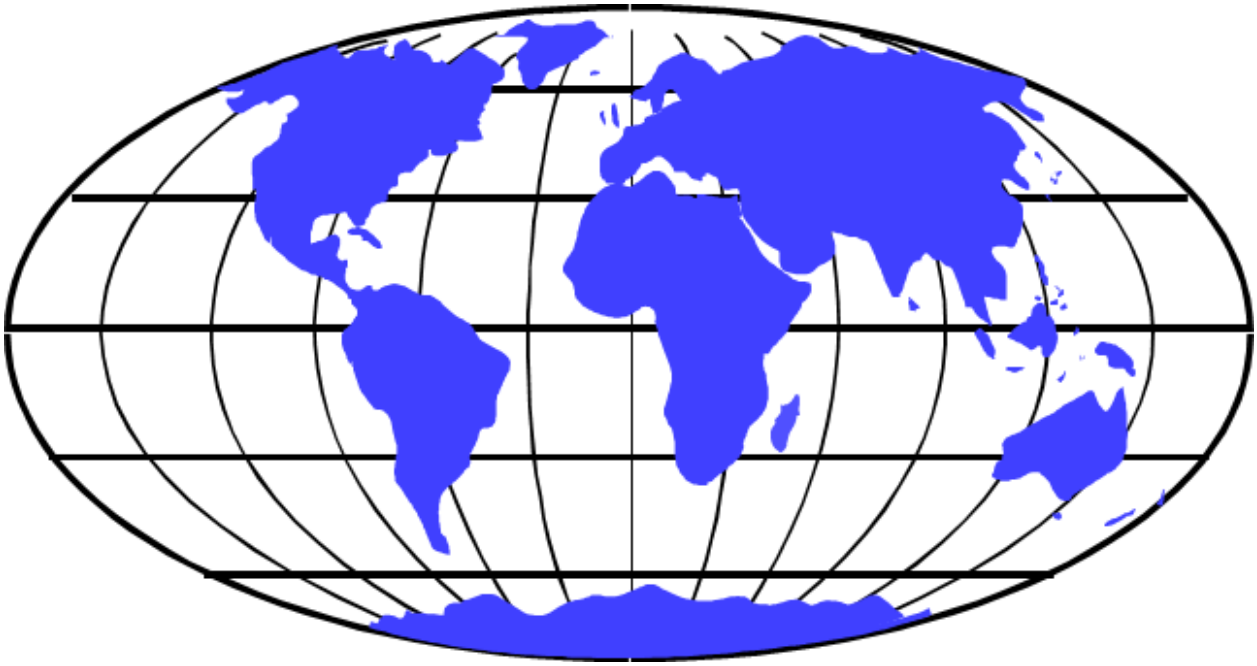
WHY MIGRATION TO 20NM BULK CMOS AND 16/14NM FINFETS IS NOT BEST APPROACH FOR SEMICONDUCTOR INDUSTRY



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1. Overview

The growth of the semiconductor industry has historically had strong dependence on the reduction in cost per transistor. The analysis of the cost per gate at 20nm, however, indicates that conventional scaling approaches for bulk CMOS have reached saturation. A similar perspective exists for the initial generation of FinFET structures at 16/14nm where cost per gate is higher than for 20nm and 28nm.

High volume applications need lower cost per transistor in order to use the new generation of process technologies. This pattern has been consistent since the development of integrated circuits. It is, consequently, appropriate to evaluate the options for continuing the pattern of lower cost per gate.

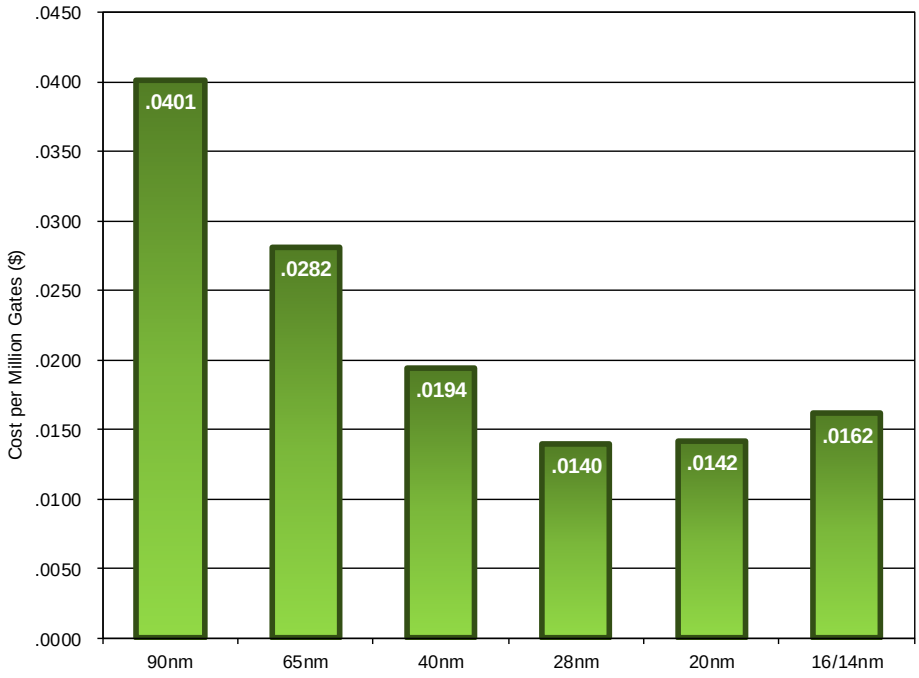
A perspective on the key factors of cost per gate levels with the reduction in feature dimensions is shown in the following table and figure.

TABLE 1
Cost per Gate Trend with Reduction in Feature Dimensions

Technology	Gates/mm^2 (KU)	Gate utilization (%)	Used gates/mm^2 (KU)	Parametric yield impact (Δ from D_0 yield)	Actual used gates/mm^2 (KU)	Gates/wafer (MU)	Wafer cost ($)	Wafer cost (Δ)	Cost per million gate ($)
90nm	637	86	546	97	532	33,831	1,357.62	--	0.0401
65nm	1,109	83	919	96	885	56,330	1,585.71	16.8	0.0282
40nm	2,139	78	1,677	92	1,538	97,842	1,898.83	19.7	0.0194
28nm	3,946	76	3,011	87	2,610	166,086	2,326.12	22.5	0.0140
20nm	6,992	65	4,524	73	3,293	209,541	2,981.75	28.2	0.0142
16/14nm	12,391	54	6,716	61	4,090	260,228	4,205.37	41.0	0.0162

Note:
* 16/14nm is in Q4/2016. 90nm, 65nm, 40nm, 28nm, and 20nm are in two years of high volume production.

FIGURE 1
Cost per Gate Trend with Reduction in Feature Dimensions



The data shows that even though there is an increase in the number of available gates with the scaling to smaller feature dimensions, it is very difficult to leverage this capability into providing lower cost per gate with the migration to 20nm bulk HKMG CMOS and 16/14nm FinFETs.

A key challenge for the semiconductor industry is to obtain high parametric yields with the reduction in feature dimensions in addition to reducing defect density. Parametric yields that are shown are based on difficulties in controlling leakage because of the problem with limitations related to doping uniformity, line edge roughness, and other physical parameters that are very sensitive to minor variations in manufacturing processes at the 20nm technology node for bulk CMOS.

To get lower leakage for bulk CMOS at 20nm, there is an increase in cost per gate. The other option is for fabless companies to accept higher leakages, which result in power consumption that is comparable to 28nm.

The need to use double patterning at 20nm also gives higher cost per wafer compared to 28nm, which further reduces the benefit of migrating to 20nm.

The migration to 16/14nm FinFETs uses the same interconnect structure as 20nm, which gives a chip area for 16/14nm that is only 5% smaller than 20nm. Lower parametric yields for 16/14nm FinFETs are due to stress control problems, overlay problems, and factors related to the step coverage and process uniformity of 3-D structures.

The impact of not reducing cost per gate is one of the most serious challenges that the semiconductor industry has faced within the last 20 to 30 years. It is, consequently, appropriate to evaluate whether other options are available that can allow scaling to 20nm and smaller feature dimensions to be effective in cost and power consumption because of the large financial impact on the semiconductor industry of not continuing with Moore's Law.

2. Approaches for Semiconductor Industry

Options for the semiconductor industry to reduce cost per gate and cost per transistor with scaling include the following:

- Adopt new device structures that can give lower leakage and lower cost per transistor.

  A key requirement is to adopt a technology that can give higher utilization of the gates that are available with the reduction in feature dimensions along with low parametric yield losses.

- Use 450mm wafers.

  In the future, 450mm wafers will be adopted, and key issues are timing and determining which technology node to commit large investments to make 450mm wafers cost effective.

  A 450mm wafer fab that can manufacture 40K WPM at 7nm will cost $12B to $14B and will need to be ramped into high volume within a short time window. Many technical challenges need to be addressed before 450mm wafers are ramped into high volume production. The analysis indicates

450mm wafers will not likely be in high volume production before 2020, other than potentially Intel at 7nm in Q4/2017. A key issue that will also need to be addressed is whether there are cost benefits to using EUV at 7nm. There is, however, uncertainty regarding when EUV will be adopted in high volume production, but EUV will not be adopted before 7nm, which is beyond the time horizon of this white paper.

The focus of the analysis is on technology options that can be used to give lower cost per gate and lower cost per transistor within the next 24 to 60 months.

Based on the analysis of multiple options that can be adopted within the industry and based on the maturity of development activities, the most likely candidate is the adoption of a fully depleted FD SOI structure.

The analysis covers 28nm, 20nm, and 16/14nm technology nodes, with feature dimensions following the conventional feature dimensions used within the semiconductor industry.

3. Wafer Cost Analysis

A perspective on wafer costs for bulk HKMG CMOS and FD SOI at 28nm and 20nm is shown in the following tables. (Note: STMicroelectronics defines their FD SOI version after 28nm as 14nm (FD14), and the next generation after that as 10nm (FD10). To simplify the comparison, a different approach is taken which can be used to give a relatively straight-forward comparison.)

TABLE 2
28nm Wafer Cost

	Bulk HKMG CMOS				FD SOI			
	Q4/2013		Q4/2014		Q4/2013		Q4/2014	
	$	%	$	%	$	%	$	%
Depreciation	1,469.54	56.36	1,376.90	55.22	1,224.15	47.53	1,147.02	46.25
Equipment maintenance	370.48	14.21	351.91	14.11	308.62	11.98	293.17	11.82
Direct labor	35.51	1.36	35.53	1.43	29.94	1.16	29.96	1.21
Indirect labor	164.65	6.31	163.63	6.56	139.60	5.42	138.74	5.59
Facilities	156.42	6.00	153.06	6.14	130.27	5.06	127.69	5.15
Wafer cost	128.95	4.95	129.97	5.21	500.00	19.41	500.00	20.16
Consumables	262.83	10.08	263.60	10.57	221.48	8.60	222.33	8.97
Monitor wafers	19.13	0.73	18.71	0.75	21.34	0.83	20.96	0.85
TOTAL Unyielded wafer cost	2,607.51	100.00	2,493.32	100.00	2,575.40	100.00	2,479.87	100.00
Line yield (%)	98.96	--	99.04	--	98.98	--	99.02	--
TOTAL Yielded wafer cost	2,634.91	--	2,517.49	--	2,601.94	--	2,504.41	--
Wafer price - 45% GPM ($)	4,790.75	--	4,577.25	--	4,730.80	--	4,553.48	--

TABLE 3
20nm Wafer Cost

	Bulk HKMG CMOS				FD SOI			
	Q4/2014		Q4/2015		Q4/2014		Q4/2015	
	$	%	$	%	$	%	$	%
Depreciation	1,822.20	57.35	1,654.19	55.78	1,482.30	49.39	1,357.49	47.73
Equipment maintenance	452.48	14.24	429.05	14.47	371.42	12.38	352.56	12.40
Direct labor	43.73	1.38	41.69	1.41	36.04	1.20	34.48	1.21
Indirect labor	208.88	6.57	203.07	6.85	170.40	5.68	166.37	5.85
Facilities	181.83	5.72	176.03	5.94	147.34	4.91	143.22	5.04
Wafer cost	128.19	4.03	128.33	4.33	500.00	16.66	500.00	17.58
Consumables	312.40	9.83	307.86	10.38	263.40	8.78	260.91	9.17
Monitor wafers	27.49	0.87	25.48	0.87	30.42	1.01	29.16	1.03
TOTAL Unyielded wafer cost	3,177.20	100.00	2,965.70	100.01	3,001.32	100.00	2,844.19	100.00
Line yield (%)	96.35	--	97.29	--	96.59	--	97.63	--
TOTAL Yielded wafer cost	3,297.56	--	3,048.31	--	3,107.28	--	2,913.23	--
Wafer price - 45% GPM ($)	5,995.56	--	5,542.38	--	5,649.60	--	5,296.79	--

Key issues in wafer costs include the following:

- The FD SOI technology that is shown in the 20nm table is called 14nm FD SOI by STMicroelectronics based on its assessment of performance and power consumption. The cost analysis is based on the FD SOI wafer cost at $500.00 for both technology options. If production volume becomes high, it is possible that this price can be reduced, which can give a further cost advantage to FD SOI.

- The wafer cost for bulk HKMG CMOS is higher than for FD SOI at 28nm, but with a relatively small difference. The key reason for the lower cost of FD SOI is the smaller number of mask and processing steps. The cost analysis is based on eight-layer metal and 3Vt levels.

  Bulk HKMG CMOS wafers at 28nm with gate last and gate first structures are in high volume production with high yields, and the cost estimate for FD SOI is based on similar production volumes.

  The FD SOI technology at 28nm can also give a lower leakage or higher performance compared to 28nm bulk HKMG CMOS, which can be used to extend the lifetime of 28nm wafer fabs.

- FD SOI at 20nm (called 14nm FD SOI by STMicroelectronics) also has lower wafer cost than bulk HKMG CMOS at 20nm and has lower power consumption and higher performance. Reasons for lower FD SOI wafer costs are the reduced number of mask levels and other processing steps compared to bulk HKMG CMOS at 20nm.

While wafer cost is an important factor, die cost is a more vital factor for most companies.

A perspective on die costs for 28nm and 20nm for bulk HKMG CMOS and FD SOI is shown in the following tables.

TABLE 4
28nm Die Cost

	Bulk HKMG CMOS				FD SOI			
	Q4/2013		Q4/2014		Q4/2013		Q4/2014	
	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2
Wafer cost ($)	2,634.91	2,634.91	2,517.49	2,517.49	2,601.94	2,601.94	2,504.41	2,504.41
Gross die per wafer	651.5	319.2	651.5	319.2	651.5	319.2	651.5	319.2
Yield (%)	76.4	59.8	78.2	61.9	79.3	61.4	80.2	63.7
Net die per wafer	497.7	190.9	509.5	197.6	516.6	196.0	522.5	203.3
Die cost ($)	5.29	13.80	4.94	12.74	5.04	13.28	4.79	12.32
Die price - 45% GPM ($)	9.62	25.10	8.98	23.17	9.16	24.14	8.71	22.39

TABLE 5
20nm Die Cost

	Bulk HKMG CMOS				FD SOI			
	Q4/2014		Q4/2015		Q4/2014		Q4/2015	
	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2
Wafer cost ($)	3,297.56	3,297.56	3,048.31	3,048.31	3,107.28	3,107.28	2,913.23	2,913.23
Gross die per wafer	651.5	319.2	651.5	319.2	651.5	319.2	651.5	319.2
Yield (%)	66.4	51.7	70.5	56.3	74.7	58.2	77.4	63.7
Net die per wafer	432.6	165.0	459.3	179.7	486.7	185.8	504.3	203.3
Die cost ($)	7.62	19.98	6.64	16.96	6.38	16.73	5.78	14.33
Die price - 45% GPM ($)	13.86	36.33	12.07	30.84	11.61	30.41	10.50	26.05

The analysis for these die costs shows the following:

- The die cost for 28nm bulk HKMG CMOS is higher than for 28nm FD SOI, with key differentiating factors being the higher yield and lower wafer costs. The leakage and power consumption of the 28nm FD SOI product are projected to be 30% lower than those of the 28nm bulk HKMG CMOS product for mainstream products. There are, consequently, benefits to use the existing 28nm wafer fab facilities to support designs with FD SOI structures as a way to extend the lifetime of the technology node.

  Trade-offs can be made between the use of bulk HKMG CMOS or FD SOI at 28nm based on cost, power consumption, and performance.

- The analysis shows that die cost for 20nm FD SOI 100mm^2 products is, however, 13.0% lower than 20nm bulk HKMG CMOS die cost in Q4/2015, which is a large cost difference for high volume mobile platforms.

  The lower die cost makes 20nm FD SOI a highly viable technology for high volume price and power consumption sensitive applications for the next 24 to 36 months. Variations such as 20nm front-end of line (FEOL) and 28nm back-end of the line (BEOL)—no double patterning required—also extends the application base that FD SOI can address. There are also other options of 20nm FEOL and 22nm BEOL, which can eliminate the need for double patterning.

- There is the projection that the power consumption of FD SOI products will be 40% lower than that of bulk CMOS products at 20nm, which is a large difference. There is also the option of having higher performance.

  The lower cost per die, decrease in power consumption, or higher performance make FD SOI an ideal solution for mobile platforms such as smartphones as well as power consumption intensive applications such as server farms.

  One compelling question is why FD SOI has not yet been adopted into the mainstream mobile computing and communications applications. The key reason is the perception that FD SOI is a high cost solution. While this concept was valid at older technology nodes, this is no longer valid with the migration to 28nm and 20nm technologies.

  Another reason proposed for not adopting FD SOI is that the semiconductor industry is migrating to 16/14nm FinFETs, with the expectation that 16/14nm FinFET structures will give lower power consumption and lower cost compared to 20nm bulk HKMG CMOS.

It is, consequently, appropriate to analyze the cost associated with the migration to 16/14nm FinFET structures, with a comparison to 14nm FD SOI (called 10nm by STMicroelectronics).

4. 16/14nm Cost Analysis

A perspective on the FD SOI and FinFET wafer costs at 16/14nm is shown in the following table.

TABLE 6
16/14nm Wafer Cost

	16nm FinFET				14nm FD SOI			
	Q4/2015		Q4/2016		Q4/2015		Q4/2016	
	$	%	$	%	$	%	$	%
Depreciation	2,480.40	58.46	2,322.58	57.97	1,728.94	49.81	1,567.93	47.97
Equipment maintenance	626.81	14.77	587.37	14.66	430.29	12.40	396.35	12.13
Direct labor	65.16	1.54	62.23	1.55	53.27	1.53	52.05	1.59
Indirect labor	293.04	6.91	280.40	7.00	210.76	6.07	206.43	6.32
Facilities	229.51	5.41	220.38	5.50	162.97	4.69	160.31	4.90
Wafer cost	138.84	3.27	135.94	3.39	520.00	14.98	520.00	15.91
Consumables	373.01	8.79	362.60	9.05	325.76	9.38	326.45	9.99
Monitor wafers	36.42	0.86	34.95	0.87	39.41	1.14	39.10	1.20
TOTAL Unyielded wafer cost	4,243.19	100.00	4,006.46	100.00	3,471.40	100.00	3,268.62	100.00
Line yield (%)	91.87	--	93.64	--	96.47	--	97.01	--
TOTAL Yielded wafer cost	4,618.69	--	4,278.57	--	3,598.42	--	3,369.36	--
Wafer price - 45% GPM ($)	8,397.62	--	7,779.22	--	6,542.59	--	6,126.12	--

The analysis of wafer costs shows the following:

- The wafer cost for 14nm FD SOI is 18.4% lower than that of the 16nm FinFET based on eight-layer metal mask levels and 3Vt levels in Q4/2016. The analysis is based on the 14nm FD SOI raw wafer cost at $520.00.

  A key factor contributing to the high cost of FinFET wafers is that of the extensive inspection steps required to ensure high yield and high reliability. A number of wafer processing steps need to be tightly controlled and monitored with the processing of FinFET structures.

- The wafer cost analysis is based on the 14nm FD SOI wafer using the same metal stack as the 16nm FinFET wafer, which is based on 64nm M1 metal pitch. The result is that gate and bit cell density should be comparable.

  The leakage of FD SOI devices is projected to be comparable to that of FinFET devices, but with the advantage of lower cost per wafer.

  To provide further visibility, the analysis of die costs for 14nm FD SOI and 16nm FinFET is shown in the following table.

TABLE 7
16/14nm Die Cost

	16nm FinFET				14nm FD SOI			
	Q4/2015		Q4/2016		Q4/2015		Q4/2016	
	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2	100mm^2	200mm^2
Wafer cost ($)	4,618.69	4,618.69	4,278.57	4,278.57	3,598.42	3,598.42	3,369.36	3,369.36
Gross die per wafer	651.5	319.2	651.5	319.2	651.5	319.2	651.5	319.2
Yield (%)	59.7	44.3	63.5	46.8	68.2	51.5	69.7	52.6
Net die per wafer	388.9	141.4	413.7	149.4	444.3	164.4	454.1	167.9
Die cost ($)	11.87	32.66	10.34	28.64	8.10	21.89	7.42	20.07
Die price - 45% GPM ($)	21.59	59.39	18.80	52.07	14.72	39.80	13.49	36.49

The yields shown for 16nm FinFETs will require major enhancements from those that are expected to be achieved in early 2015 and are potentially high. The analysis shows that the 14nm FD SOI die is 28.2% lower than 16nm FinFET die cost (100mm^2 die) in Q4/2016, which is a large difference.

Large investments are being made in 16/14nm FinFET wafer processes and in establishing large wafer capacity based on the expectations that devices will have low power consumption or high performance and customers will be willing to pay price premiums for these benefits. These expectations are likely to be overly optimistic within high volume mobile platform applications. It is, however, possible that within data infrastructure applications, there will be the willingness to pay the price premiums for the lower power consumption if the options are 16nm FinFETs and 20nm bulk CMOS.

The key requirement for FD SOI is to establish supply chains that can support the participation in high volume end markets. There is the expectation that this will occur. Another possibility is that FD SOI can be scaled to 10nm (called 7nm by STMicroelectronics), which will provide an additional technology node for this capability, but this possibility needs further analysis.

There are clearly compelling reasons to utilize FD SOI as an alternative to the legacy bulk CMOS technology and emerging FinFET structures based on three generations of technology, ie, 28nm, 20nm (called 14nm by STMicroelectronics), and 14nm (called 10nm by STMicroelectronics).

It is clear that FinFET (or Tri-Gate) structures will be needed for the support of migration to 7nm and potentially 5nm technology nodes. Intel has demonstrated the power consumption advantage of its Tri-Gate structures at 22nm, especially with its second-generation designs at 22nm such as Haswell. ***Intel, however, has leading design and design-for-manufacturing technologies, which will be difficult for the foundry-fabless industry to replicate in the next 24 to 36 months.*** Intel is also in its second-generation Tri-Gate technology at 14nm, but this is a new technology node for others. Intel, however, has postponed the ramp-up of its 14nm Tri-Gate structures by one quarter, and this is a key indicator of the manufacturing complexity of 3-D structures at the 16/14nm technology node.

While it is important for the foundry environment to track Intel, it is more important to provide the best combination of cost, power consumption, and performance. Technology roadmaps need to be established based on business metrics in addition to technical metrics.

5. Strategic Issues within FD SOI Supply Chain

Strategic issues within the FD SOI supply chain include the following:

- Working products with FD SOI at 28nm have been demonstrated by STMicroelectronics with significant performance and power consumption advantages compared to bulk CMOS. Products produced by STMicroelectronics are complex and demonstrate the ability to manufacture large area devices in FD SOI.

- Three companies, which are Soitec, SunEdison, and Shin-Etsu Handotai (SEH), are supplying FD SOI wafers. The supply chain for FD SOI wafers can be expanded rapidly to provide the required wafer capacity if a demand environment is established.

- The use of body biasing provides significant performance and power consumption advantages for FD SOI. Body-biasing methodologies for FD SOI can use EDA tools that have been developed for bulk CMOS technology. Also, design flows for FD SOI are effectively identical to those for bulk CMOS.

- Libraries and basic IP developed for bulk CMOS can be easily modified for FD SOI. The cost of modification between bulk CMOS and FD SOI is approximately 10% of that required to migrate to a new technology node for bulk CMOS at 20nm.

- Industry standard feature dimension metrics are used in this white paper for the comparison of technologies, and an example is that gate feature dimensions of 20nm FD SOI are similar to those of 20nm bulk CMOS. Both options use the same BEOL structures.

  The 14nm FD SOI technology shrinks the gate feature dimension from 20nm but uses the 20nm BEOL structure. The 14nm FD SOI option (called 10nm by STMicroelectronics) is compared to 16/14nm FinFETs.

  While the cost comparison at these technology nodes provides important insight, it is also essential for the timeline of high volume ramp-up for each option to be close to one another.

There are many advantages for FD SOI to be widely adopted for high volume, low cost, and lower power applications in the future. It is important for the semiconductor industry to be willing to make investments to provide optimum solutions to its customers rather than follow the roadmap of a specific company. Being short-term focused and not willing to adopt new concepts can have large cost penalties within the foundry-fabless environment.

The semiconductor industry has not grown to be a $300B industry by not utilizing the best technology that is available.

6. Conclusion

- The roadmap being followed by the mainstream semiconductor industry, which is the migration from bulk CMOS at 28nm to 20nm followed by the migration to 16/14nm FinFETs, does not provide a reduction in cost per transistor unless there are extensive efforts made to increase parametric yields. This can delay the ramp-up of high volume production, where design costs for a complex product can be $0.75B to $1.00B.

  Cost penalties resulting from very high design costs and long time-to-market can have a serious impact on the competitiveness of semiconductor vendors that select this approach. Semiconductor companies that are participating in fast-moving markets cannot tolerate the additional costs of design and long time-to-market associated with trying to fine-tune technologies that are inherently high cost.

- The analysis of the wafer cost and yielded die cost for FD SOI shows the following for 100mm^2 die:
  - The die cost of 28nm FD SOI is 3.0% lower than the 28nm bulk CMOS die cost.
  - The die cost of 20nm FD SOI is 13.0% lower than the 20nm bulk CMOS die cost.
  - The die cost of 14nm FD SOI is 28.2% lower than the 16nm FinFET die cost.

- The lower power consumption and higher performance of FD SOI compared to 28nm and 20nm bulk CMOS give major competitive advantages in high volume portable applications.

- The lower cost of FD SOI die compared to 16nm FinFET die provides an overwhelming advantage to utilizing FD SOI at this technology node.

  It is probable that there are advantages to utilizing FinFET at 10nm and 7nm, but these decisions can be made by foundry-fabless companies in 2015 or 2016. The key requirement is how to satisfy the needs of smartphones and other mobile platforms for low cost and low power volume manufacturing in 2015, 2016, and 2017.

- There is the need to build up the supply chain and ecosystem for FD SOI, which includes libraries and IP, but these costs are relatively low compared to the financial benefits that can be obtained by semiconductor vendors that have high volume products. There is the perspective that EDA tools developed for bulk CMOS can be easily adapted to FD SOI.

  Deviating from mainstream roadmaps has had dramatic financial penalties in the past, but it is likely that being overly committed to mainstream roadmaps will result in large financial penalties in the future.

Options for the migration to 20nm, 14nm, and 10nm technology nodes need to be based on cost, power consumption, and performance metrics that can be easily verified.

Biography

Handel Jones is the founder and CEO of International Business Strategies, Inc. (IBS), which is based in Los Gatos (California) and has been in business for 25 years. IBS is active in quantifying the cost of implementing and manufacturing IC designs and financial metrics related to market positioning. IBS provides support to many global leaders in key areas of technologies, markets, and business strategies for the semiconductor and electronics industries.

Handel Jones is also the author of *Chinamerica*, which was published by McGraw-Hill and provides insight into the drivers for the economies of the U.S. and China.