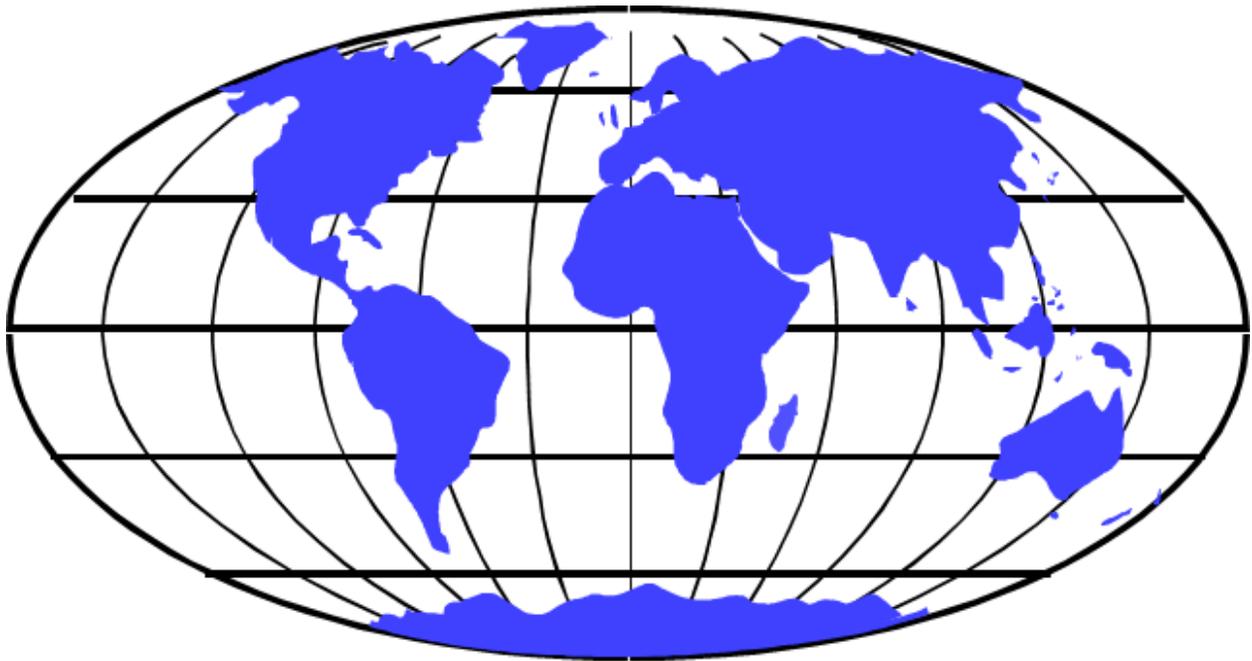


# *IBS*

## **CALIBRE: THE GOLDEN STANDARD FOR PHYSICAL VERIFICATION**

---



Dr. Handel Jones  
Founder and CEO, IBS, Inc.  
Los Gatos, California

White Paper  
August 2012

**International Business Strategies, Inc.**  
632 Industrial Way • Los Gatos, CA 95030 • USA  
Phone (408)395-9585 • Fax (408)395-5389  
[www.ibs-inc.net](http://www.ibs-inc.net) • [info@ibs-inc.net](mailto:info@ibs-inc.net)

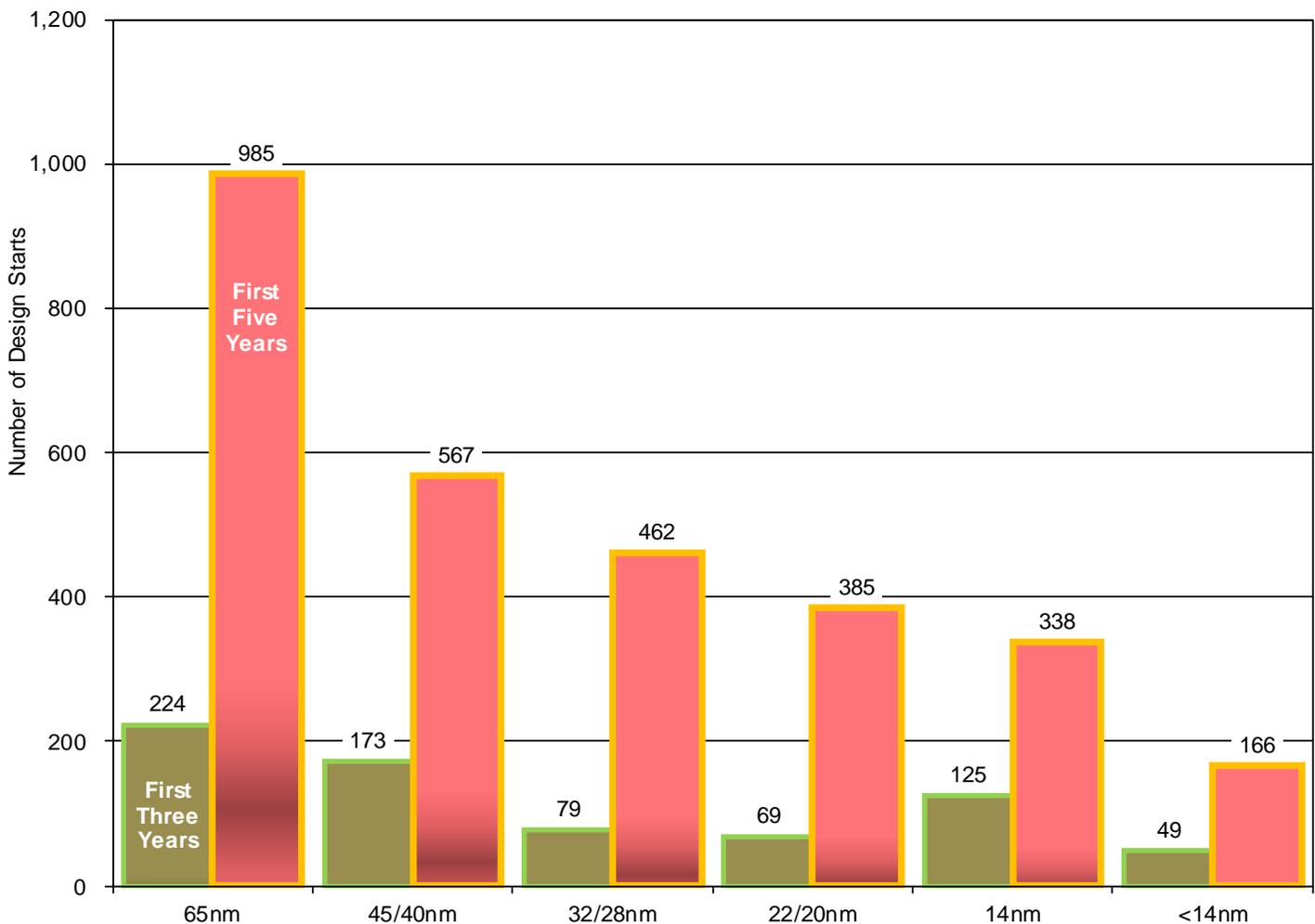
## Introduction

Ramping up new generations of process technologies requires very close coupling between the physical design implementation steps and processing parameters. There is the analysis of problem areas and benefits that Calibre provides to the design and wafer processing communities.

### 1. Overview of Design Environment

The semiconductor design environment is going through a number of changes with the reduction in feature dimensions, and one area is that the number of designs shows a steady decline as feature dimensions shrink. A perspective is shown in the following figure.

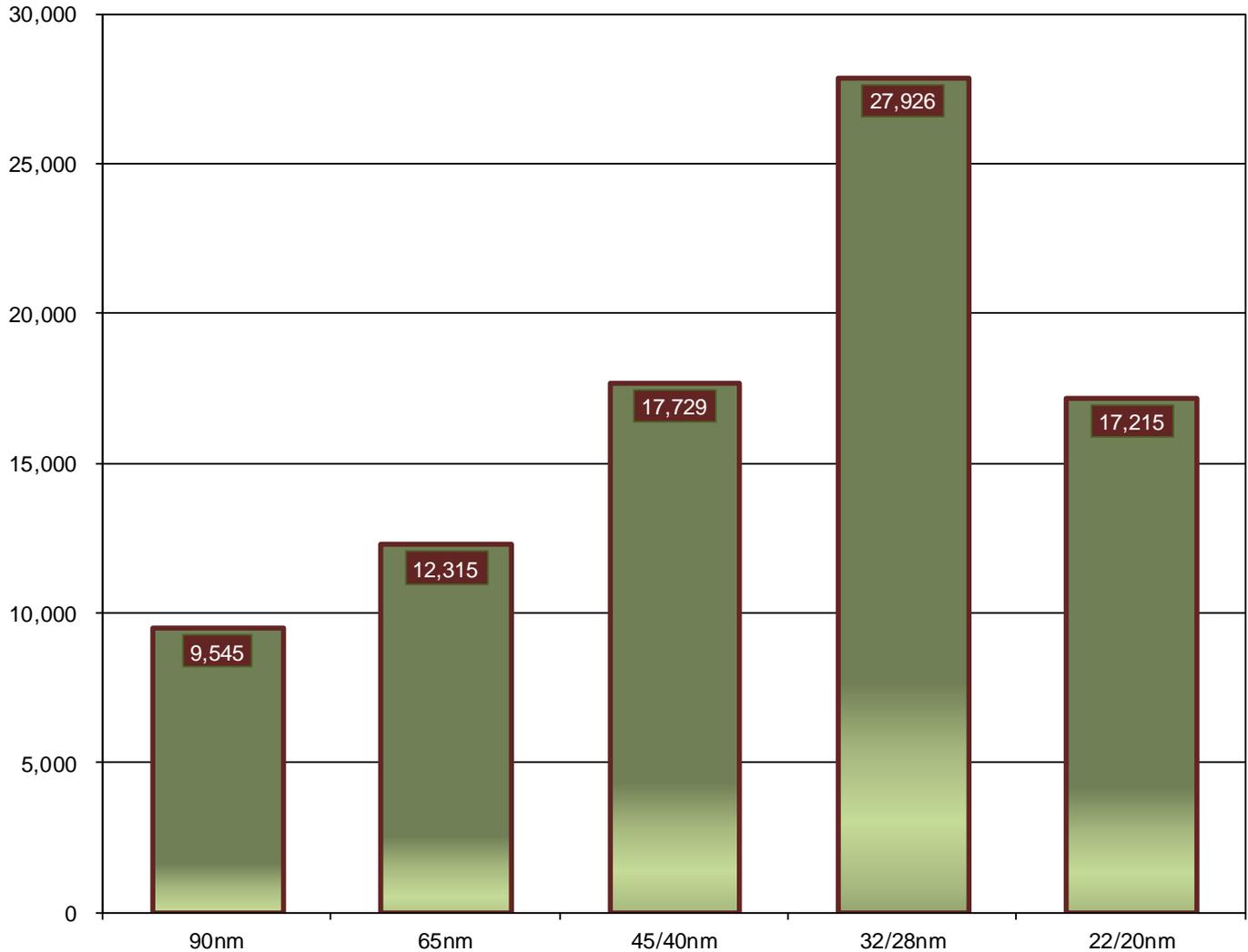
FIGURE 1  
Number of Advanced Feature Designs (Initial Years)



The reduction in the number of designs is due to both increased IP integration and the impact of higher design costs. As more IP is integrated, a smaller number of IC products are needed within systems. The increase in design costs results in a reduction in the number of companies that have the financial resources to implement the designs.

The revenue value per design, however, increases as feature dimensions shrink, and a perspective on foundry revenues by feature dimension during the first five years of a technology node is shown in the following figure.

FIGURE 2  
Foundry Revenues by Feature Dimension for First Five Years



The revenues by technology node increased for 90nm through 32/28nm, but with a decline at 20nm because of a slowing in the reduction of cost per gate. If there are technology breakthroughs at 20nm, this trend can change.

The 14nm revenues are not included because the first five years extends beyond the market window that can be analyzed.

With the reduction in the number of designs and increase in revenues per technology node, revenues per design increase from \$125M at 65nm to \$493M at 32/28nm.

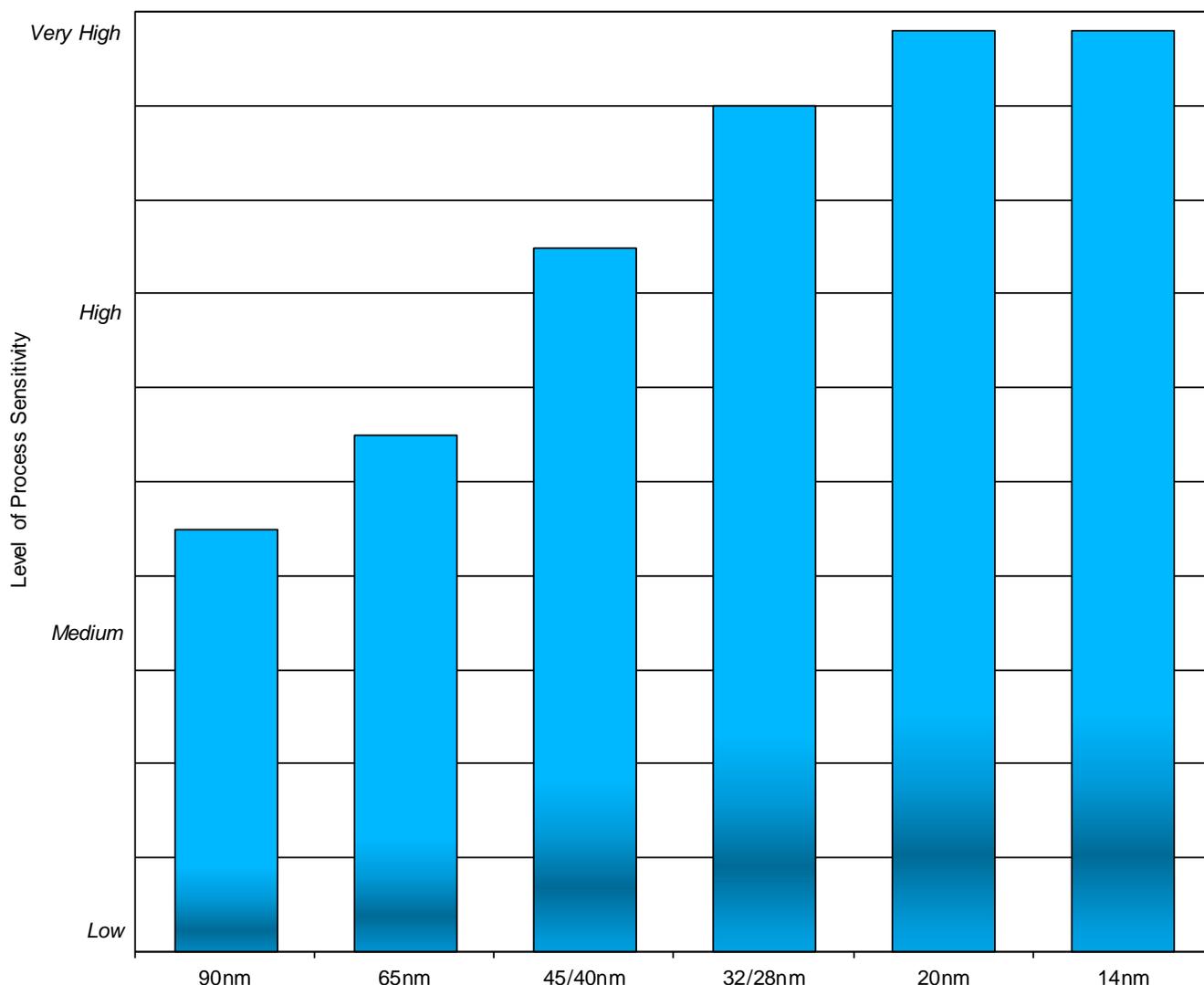
The increased revenues per design as feature dimensions shrink combined with the very high costs associated with re-spins places very high importance on first-time success in silicon for new products.

Obtaining high probability of first-time success in silicon requires parametric yields to be at expected levels as well as designs to not have functional problems. Checking for electrical as well as physical design problems becomes increasingly important, even with the perspective that the costs associated with checking increase rapidly as feature dimensions shrink. Re-spin costs can be \$20M to \$50M in addition to the impact of delays on time-to-market, which also increases the need for thorough and accurate physical verification.

## 2. Process Sensitivity

As feature dimensions shrink, there is an increase in the relative process sensitivity of designs, a perspective of which is shown in the following figure.

FIGURE 3  
Relative Level of Process Sensitivity



Process sensitivity is defined as the impact of variations in process parameters on design functionality, which include the following:

- Transistor: Includes poly and other critical feature dimension tolerances
- M1: Includes metal pitch, contact resistance, RC-related delays, transmission line effects, etc
- M2 through Mn: Includes metal-to-metal cross coupling parasitics as well as variations in feature dimensions

Each of the above areas becomes more sensitive to process variability as feature dimensions are reduced. There is also the need to evolve from the 2-D to 3-D domains for modeling, parameter extraction, DRC, etc.

At the older generations of technology, the transistor structures controlled the performance of most products, but at the smaller feature dimensions such as 28nm and 20nm, it is the interconnect structures that have the largest impact on performance for many designs.

Variations in metal pitch, metal thickness, lithography patterns based on OPC, RET, etc, can significantly affect the delays associated with interconnect structures. In addition to the absolute values, there is also an increase in the variability of the values, which can result in large parametric yield losses.

Design verification, consequently, becomes increasingly important as feature dimensions shrink and design complexity increases. The design verification steps include the following:

- Functional verification: Includes simulation, acceleration, emulation, etc. These steps were not closely connected with the physical implementation of digital designs in the past, but this is changing.
- Physical verification: Includes the impact of reticles and process variations. This area has become highly critical at 28nm and will be even more important at 20nm in order to ensure that designs meet their performance requirements.

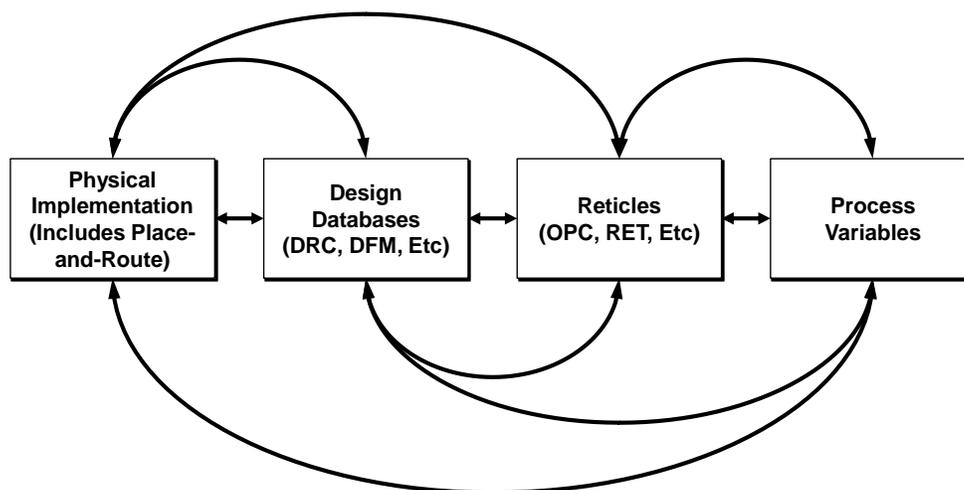
To obtain timing closure, IC vendors are being forced to increase the size of the teams committed to physical implementation and verification.

While adding engineers can be a short-term fix, the real need is to use the best tools available, provide access to high levels of computer power, and ensure that design engineers are trained in the use of the tools. There is also the need to bridge the databases for designs with those for reticles and wafer processes.

Design tool selection and optimization for physical design and verification of use will become a more important differentiation between companies that complete their designs within the projected cost and time budgets and those that face weakening market share positions.

### 3. Link Between IC Design and Manufacturing

FIGURE 4  
Link Between IC Design and Manufacturing



The physical implementation of designs requires that manufacturing- and yield-aware capabilities be established and built into the physical design verification steps. The OPC and RET capabilities that are used as well as the lithography printing steps need to be closely coupled with the physical verification steps. Physical verification capabilities, such as those provided by the Calibre family, need to be part of the product lifecycle ecosystem.

Establishing the appropriate bridging technologies between design and manufacturing requires access to the appropriate EDA tools as well as the operating environment where tools are efficiently used. Design engineers within the fabless/foundry environment must gain access to the skill sets that are common among IDMs, and expertise in using the appropriate tools is a critical step in this arena.

### 4. Solutions Used in IC Industry

The analysis of activities of leading foundry vendors shows that the various versions of Calibre are used as the “Golden Sign-off Environment”. Calibre is used by all of the foundry vendors for the sign-off of new processes, including 28nm and 20nm, and the reasons include the superior verification capabilities that are built into Calibre for advanced feature and 3-D structures.

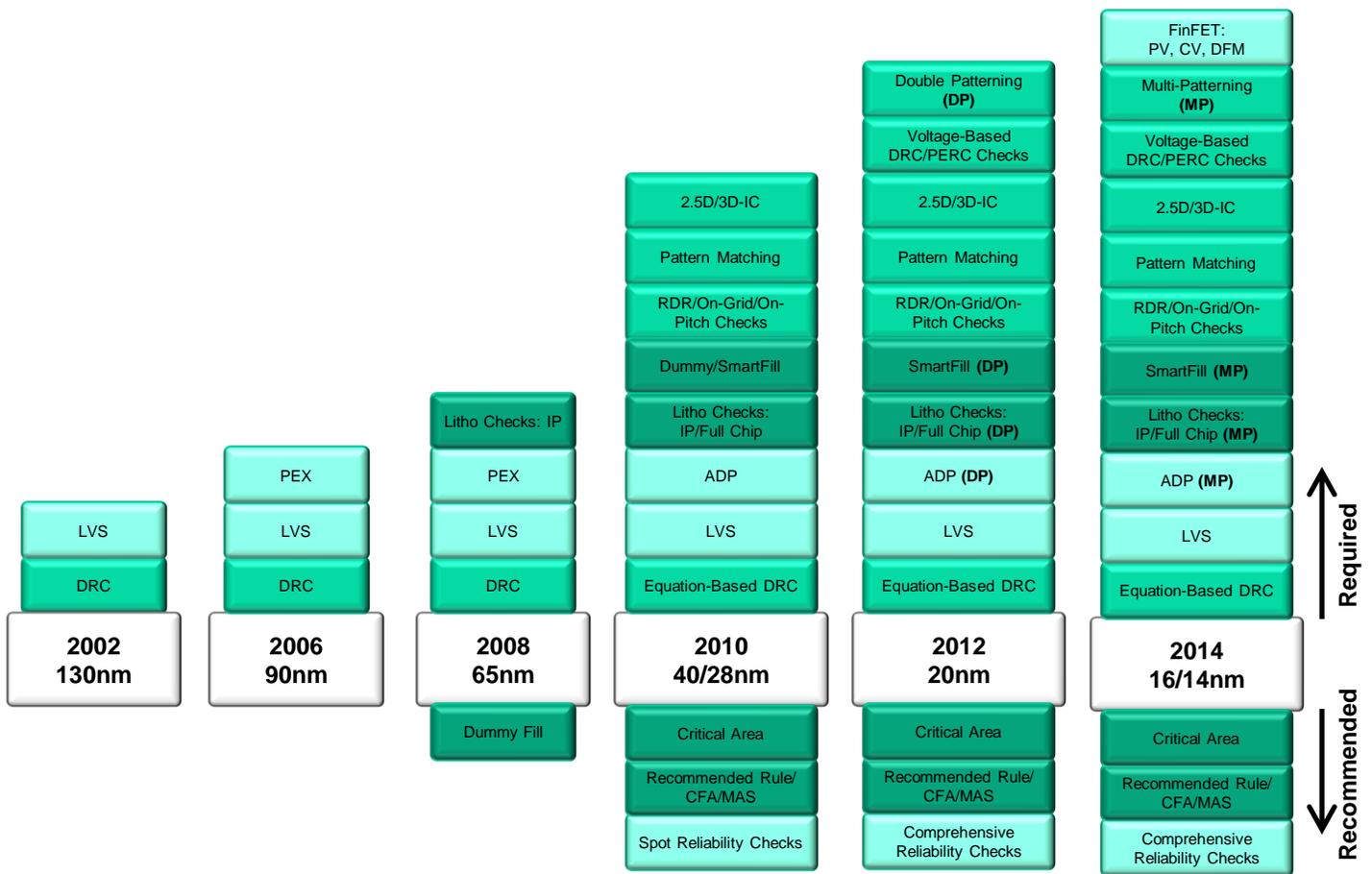
The Calibre PV rule check data is developed by foundry vendors as new processes are stabilized. The data is systematically upgraded as additional process expertise is developed through the initial volume production phase. This feedback mechanism continuously improves the quality of the Calibre environment and gives high probability that the designs will operated as expected.

There is also extensive use of Calibre by the fabless companies that utilize the foundry vendors. The analysis shows that over 80% of IC companies are using Calibre for design sign-off and as feature dimensions are reduced, the percentage increases.

A further metric of the broad use of Calibre is its 69% market share for physical verification on an overall basis, with market share approaching 80% for the advanced technology nodes.

A perspective on Calibre's features and how they have been enhanced as advanced feature dimensions are reduced is shown in the following figure.

FIGURE 5  
Calibre Feature Expansion With Reduction in Feature Dimensions



The migration to smaller feature dimensions involves the need to address process steps such as double-, triple-, quad-patterning, etc, and these requirements are supported by Calibre.

The adoption of FinFETs will involve a range of new technology factors that must be supported, and it is important to address these factors at the embryonic phase of process development and continuously enhance them as the process experience is expanded.

The technology of 3-D packaging is another new area that will be increasingly important, and Calibre is already supporting many of these requirements.

The increased capabilities within Calibre that are driven by the reduction in feature dimensions combined with the close relationship with the wafer manufacturing facilities (eg, new process technologies being developed) make Calibre a very compelling tool for the IC design and process development support.

The collaboration with foundry vendors and technology leaders allows Calibre to support IC vendors during the lifecycle of the technology nodes, ie, from initial stage through multiple variants during the high-volume phase.

While the legacy approach to IC design has been to implement the physical design steps and fix DRC problems after routing is completed, the large increase in the number of fixes necessary is making this option unacceptable.

At 28nm and 20nm, DRC constraints must be built in during the physical design and DFM implementation steps. Automatic fixing of design rule violations is necessary and must be done at the IP, block, and chip levels in real time. The analogy is that of zero defects during each step of the manufacturing process for electronics equipment. By having Calibre as the “Golden Sign Off” standard, it is appropriate to also use Calibre during the physical implementation steps.

The OPC, RET, and metal fill requirements for CRM must also be part of the design rule violation checking and fixing. These requirements must also be addressed during the physical design implementation steps, and Calibre capabilities are consistent with these needs.

The close partnerships that need to be developed between IC design teams and foundry vendors at 28nm, 20nm, and 14nm can be implemented by the use of EDA tools that are widely adopted by both areas. The value for IC and foundry vendors from better DRC and DFM technologies is very high in terms of reducing product lifecycle costs, where the variations in physical parameters have to be included as part of the design flow.

Activities during the physical design implementation increasingly affect IC product yields, performance, power consumption, and product lifecycle costs. A penalty of 10% to 20% increase in verification costs that improve product yields can translate into 10X or 20X payback from lower product lifecycle costs.

Improving yields by 5% can reduce product lifecycle costs by hundreds of millions of dollars for some high-revenue products.

Having a high probability of first-time success in silicon, which includes designs operating as expected from a functional perspective as well as achieving expected performance levels, has payback potential of billions of dollars for products in the smart phone and tablet computer markets.

Calibre and its derivatives are well-positioned to provide a high level of value to IC vendors from a business as well as technology perspective. In addition to adopting the Calibre family, there is the need to develop high levels of expertise in using the tools.

The automated fixing of violations of physical parameters during the routing steps will also become a “must have” capability for the 20nm and 14nm designs. Using Calibre with its broad-based adoption is an efficient way to address the increasing challenges of physical design.

## **Conclusion**

The benefits of Calibre are not only evident during the design implementation steps but also have a major impact on reducing product lifecycle costs and strengthening the performance and power consumption of the end products.

## Biography

Handel Jones is the founder and CEO of International Business Strategies, Inc. (IBS), which is based in Los Gatos (California) and has been in business for 24 years. IBS is active in trading advanced technology development, including 20nm, 14nm, and future generations. The company is also active in the design of complex semiconductor products including cost and design productivity models. IBS provides support to many global technology leaders in key areas of semiconductor technologies, markets, and business strategies.

Handel is also the author of *Chinamerica*, which was published by McGraw-Hill and provides insight into the drivers for the economies of the U.S. and China.